What is claimed is:

1. A process for fabricating an electrical circuit, wherein successive layer treatments are carried out on top of a substrate in order to produce at least a first component in a first portion of the circuit and second components in a second portion of the circuit adjacent to the first portion, wherein at least a first of the layer treatments comprises the following steps:

- forming, in a first electrically insulating material present on top of the substrate, compensation cavities in the first portion of the circuit and trenches corresponding to at least some of the second components in the second portion of the circuit;
- covering the first insulating material with a first conducting material so as to substantially fill the compensation cavities and the trenches formed in the first insulating material;
- polishing the first conducting material until exposing part of the first insulating material in the second portion; and
- removing the first conducting material in the first portion;

and wherein at least a second of the layer treatments comprises the following steps:

- forming, in a second electrically insulating material present on top of the substrate, at least one trench corresponding to the first component in the first portion of the circuit;
- covering the second insulating material with a second conducting material so as to substantially fill the trench formed in the first portion; and
- partially removing the second conducting material until exposing part of the second insulating material in the first portion.

2. The process according to Claim 1, wherein said first layer treatment is carried out before said second layer treatment, the second insulating material being deposited on top of the first insulating material.

3. The process according to Claim 2, wherein at least a third of the layer treatments comprises the following steps:

- forming, in a third electrically insulating material present on top of the substrate, trenches corresponding to second components in the second portion of the circuit;

- covering the third insulating material with a third conducting material so as to substantially fill the trenches formed in the third insulating material;

- polishing the third conducting material until exposing some of the third insulating material in the second portion, in such a way that the surface of the third insulating material becomes higher in the first portion than in the second portion;

- etching first cavities in the third insulating material in the first portion of the circuit in such a way that the first cavities have their bottoms deeper than the level of said surface of the third insulating material in the second portion of the circuit,

wherein said first layer treatment, carried out after said third layer treatment, starts with a step of depositing the first insulating material in the form of a layer covering the third insulating material in the first and second portions of the circuit so that the surface of the first insulating material has second cavities conforming substantially to the first cavities and constituting said compensation cavities.

4. The process according to Claim 1, wherein the partial removal of said second conducting material comprises polishing, chemical etching by means of a liquid solution or dry plasma etching.

5. The process according to Claim 1, wherein the cavities formed in the first insulating material are shallower than the trenches formed in the first insulating material.

6. The process according to Claim 1, wherein the removal of said first conducting material in the first portion comprises a step using chemical etching by means of a liquid solution or dry plasma etching.

7. The process according to Claim 5, wherein the removal of said first conducting material in the first portion comprises a polishing step.

8. The process according to Claim 1, wherein, during said second layer treatment:

- compensation cavities are furthermore formed in said second insulating material; and
- the compensation cavities formed in said second insulating material are substantially filled with the second conducting material;

and wherein said second layer treatment furthermore includes, after the partial removal of the second conducting material, a removal of the second conducting material from the compensation cavities that are formed in said second insulating material.

9. The process according to Claim 8, wherein the removal of the second conducting material from the compensation cavities that are formed in said second insulating material is carried out by masking the trench corresponding to the first component.

10. The process according to Claim 8, wherein the removal of the second conducting material from the compensation cavities that are formed in said second insulating material comprises chemical etching by means of a liquid solution or dry plasma etching.

11. The process according to Claim 8, wherein the compensation cavities formed in said second insulating material are formed simultaneously with the trench corresponding to the first component.

12. The process according to Claim 8, wherein, during said second layer treatment, trenches corresponding to at least some of the second components are furthermore formed in said second insulating material in the second portion of the circuit, and wherein the partial removal of the second conducting material is carried out so as to furthermore expose a part of the second insulating material in the second portion.

13. The process according to Claim 12, wherein the removal of the second conducting material from the compensation cavities that are formed in said second insulating material is carried out by masking the trench corresponding to the first component and the trenches corresponding to at least some of the second components.

14. The process according to Claim 1, wherein said first component is an inductor, an antenna, a high-speed electrical signal transmission line, or a capacitor.

15. The process according to Claim 1, wherein said first and/or second electrically insulating materials deposited as respective layers are polished before the formation of the compensation cavities and the trenches in each of said first and/or second insulating materials, respectively.

16. The process according to Claim 1, wherein said first and/or second electrically insulating materials are deposited in the form of respective layers each having a plane upper surface at the end of the deposition of each of said first and/or insulating materials.

17. A circuit fabrication process wherein a first layer of treatments comprise the steps of:

forming, in a first insulating material present on a substrate:

(i) compensation cavities in a first portion of a circuit, and

(ii) trenches corresponding to components in a second portion of said circuit;

filling substantially said compensation cavities and said trenches with a first conducting material;

polishing said first conducting material to expose said first insulating material in said second portion; and

removing said first conducting material in said first portion; and

wherein a second layer of treatments comprises the steps of:

forming, in a second insulating material present on said substrate, a trench corresponding to a component in said first portion;

filling substantially said trench formed in said first portion with a second conducting material; and

removing partially the second conducting material until exposing part of the second insulating material.

18. The process according to Claim 17 wherein said second insulating material is deposited on top of said first insulating material.

19. The process according to Claim 18 wherein said first layer treatment is carried out after a third layer treatment and further comprises the step of depositing said first insulating material in the form of a layer covering a third insulating material in said first and second portions of said circuit where said surface of said first insulating material has cavities conforming substantially to said first cavities and constituting said compensation cavities.

20. The process according to Claim 19 wherein a third of layer treatment comprises the steps of:

forming, in said third insulating material present on said substrate, other trenches corresponding to other components in said second portion of the circuit;

filling substantially said other trenches with a third conducting material;

polishing said third conducting material to expose said third insulating material in said second portion such that the surface of said third insulating material is higher in said first portion than in said second portion; and

etching other cavities in said third insulating material in said first portion of said circuit in such a way that said first cavities have their bottoms deeper than the level of said surface of said third insulating material in said second portion of said circuit.

21. The process according to Claim 17, wherein partial removal of said second conducting material comprises one of polishing, chemical etching, and dry plasma etching.

22. The process according to Claim 17, wherein said first insulating material cavities are shallower than said first insulating material trenches.

23. The process according to Claim 17, wherein said removal of said first conducting material in said first portion comprises at least on of the step of etching by means of one of a liquid solution and dry plasma etching.

24. The process according to Claim 23, wherein the removal of said first conducting material in the first portion comprises a polishing step.

25. The process according to Claim 17, wherein, during said second layer treatment compensation cavities are formed in said second insulating material, which are substantially filled with the second conducting material, and wherein said second layer treatment furthermore includes, after partial removal of the second conducting material, the step of removing said second conducting material from said compensation cavities that are formed in said second insulating material.

26. The process according to Claim 25, wherein said removal of said second conducting material from said compensation cavities formed in said second insulating material comprises either one of the steps of masking said trench corresponding to said first component, and chemical etching by means of a liquid solution or dry plasma etching.

27. The process according to Claim 25, wherein said compensation cavities are formed simultaneously with said trench corresponding to said first component.

28. The process according to Claim 25, further comprising the step of forming, during said second layer treatment, trenches corresponding to at least some of said second components in said second insulating material in said second portion, wherein said partial removal of said second conducting material is carried out so as to furthermore expose part of said second insulating material in said second portion.

29. The process according to Claim 28 wherein the removal of the second conducting material from the compensation cavities in said second insulating material includes the step of masking ones of said trenches corresponding to said first and second components.

30. The process according to Claim 17, wherein said first component is one of an inductor, an antenna, a high-speed electrical signal transmission line, and a capacitor.

31. The process according to Claim 17, wherein at least one of said first and second electrically insulating materials deposited as respective layers are polished before the formation of said compensation cavities and said trenches in each of at least one of said first and second insulating materials.

32. The process according to Claim 17, wherein at least one of said first and second electrically insulating materials are deposited in respective layers each having a plane upper surface.